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D5.1 - DESCRIPTION AND METHODOLOGY OF EVALUATION OF INITIAL POCS

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TABLE OF CONTENTS

FIGURES

TABLES

ABBREVIATIONS

Acronym	Description
AAL	Antenna array-like
AD	Analog devices
AI	Artificial intelligence
AO	Alternate optimization
AP	Access point
BACKCOM	Backscatter communication
BCD	Block coordinate descent
BS	Base station
CCA	Clear channel assessment
CCU	Central connectivity unit
COT	Channel occupancy time
CR	Constraint relaxation
CSI	Channel state information
CW	Continuous wave
DC	Dual connectivity
DL	Deep learning
DMA	Dynamic metasurface antenna
DUT	Device-under-test
EM	Electromagnetic
EW	Electronic warfare
ETSI	European Telecommunications Standards Institute
FDMA	Frequency division multiple access
FPGA	Field programmable gate array
HC	High-capacity device
IEEE	Institute of Electrical and Electronics Engineers
IO	Indoor office
IOT	Internet-of-things
ISM	Industrial, Scientific and Medical
KKT	Karush-Kuhn-Tucker
LA	Latency aware
LOS	Line-of-sight
MAC	Medium Access control
MIMO	Multiple-input multiple-output
MISO	Multiple input single output
ML	Machine learning
MSE	Mean square error
N-RIS	Non-reconfigurable intelligent surface
NLOS	Non-line-of-sight
NOMA	Non orthogonal multiple access
OFDM	Orthogonal frequency division multiplexing

PER	Packet error rate
PoC	Proof of Concept
PSR	Packet success ratio
PDP	Power-delay profile
QAM	Quadrature amplitude modulation
SOTA	State of the art
RSSI	Received signal strength indicator
SDR	Software defined radio
SNR	Signal to noise ratio
SoTA	State-of-the-art
SW	Software
TC	Technology component
TCF	Temporal correlation function
VNA	Vector network analyser

EXECUTIVE SUMMARY

Deliverable 5.1 is the first deliverable of WP5, where the proof of concept (PoC) demonstrations of selected 6G-SHINE technologies is developed. D5.1 takes input from Task 5.1 of the project, “Detailed presentation of the technology components to be demonstrated”. In this task, each PoC is designed according to a commonly agreed methodology, taking into account its expected relevance in the context of 6G-SHINE project, the hardware and software capabilities of the testbed platforms available at the partners’ premises, and the feasibility of implementation within the project time. Relevant key performance indicators (KPIs) are also defined for each PoC.

In this deliverable, we introduce the agreed methodology for PoC development, followed by a description of each envisioned PoC. The PoCs presented in this deliverable are listed below, along with their connection to the respective technology components (TCs) defined in the 6G-SHINE project proposal:

- Low latency channel emulator (addressing TC2)
- Latency aware MAC access (addressing TC11)
- Jamming resilient PHY (addressing TC6)
- Intra-subnetwork macro-diversity (addressing TC8)
- Centralized RRM (addressing TC13)
- Centralized/distributed interference management (address both TC12 and TC13)
- Jamming detection using anomaly detection (addressing TC15)

For each PoC, we present the envisioned architecture, hardware and software requirements, applicable KPIs and targeted demonstration scenario.

1 INTRODUCTION

The main objective of WP5 in 6G-SHINE is to implement and evaluate over software and/or hardware platforms selected relevant technology components (TCs) defined in the project, in order to assess their validity in laboratory and provide feedback to WP2/WP3/WP4 on the capabilities of their designed technologies of achieving the expected performance.

WP5 addresses indeed objective 8 of the project, i.e. *Validate the most promising technology components via proof-of-concepts in laboratory facilities.*

Since 6G-SHINE encompasses a very broad set of technologies, ranging from physical layer solutions to architectural enhancements, in WP5 we focus only on a subset of the 16 TCs studied in the other technical WPs. This subset is identified based on their expected promise according to the preliminary studies carried out in the other WPs, as well as the feasibility of their implementation within the project time. It is worth to recall that 6G-SHINE is a low technology readiness level (TRL) project (1-4), and we do not aim at integrating all the innovations in the project in a large PoC, but rather focus on smaller PoCs dedicated to the selected TCs. Integrated PoCs will rather be object of a Phase 2 project of the SNS work programme.

The work in WP5 addresses the following TCs defined in the 6G-SHINE proposal:

TC2. Channel models for in-X scenarios
TC6. Jamming-aware native PHY design
TC8. Intra-subnetwork macro-diversity
TC11. Latency-aware access in the unlicensed spectrum
TC12. Centralized radio resource management
TC13. Distributed/hybrid radio resource management.
TC15. Hybrid management of traffic, spectrum and computational resources

We target a TRL equal to 4 (Technology validated in lab) for the selected technologies. The list of defined PoCs is presented in Table 1, along with the responsible project partners, the corresponding TC, and the WP where the TC is studied.

TABLE 1. LIST OF 6G-SHINE POCS.

Number	Lead partner	Title	TC	WP
1	Keysight	Low latency channel emulator	TC2	WP2
2	IMEC	Latency Aware MAC access	TC11	WP3
3	IMEC	Jamming resilient PHY	TC6	WP3
4	FHG	Intra-Subnetworks macro-diversity	TC8	WP3
5	Bosch	Centralized RRM	TC13	WP4
6	COGN	Centralized/Distributed interference management	TC12, TC13	WP4
7	IDE	Jamming detection using Anomaly detection methods	TC15	WP4

Section 2 introduces the methodology adopted for PoC definition and evaluation. A description for each of the seven PoCs is then presented in section 3. In particular, the high-level architecture of the targeted demonstration is described, along with the hardware software requirements, applicable KPIs, and demonstration scenarios. Concluding remarks are presented in section 4.

2 METHODOLOGY OF POC DEFINITION AND EVALUATION PROCESS

Defining what is a proof of concept and what is the process to evaluate its offered performance or functionality is not a trivial task, as it highly depends on its nature (HW/SW component) and its intended use. The definition will depend on what kind of system it will be part of, and on how to tackle or avoid possible integration problems. In order to unify as much as possible our approach within the project, while taking into account the diverse nature of the TCs developed, we adopted the following approach, illustrated in Figure 1.

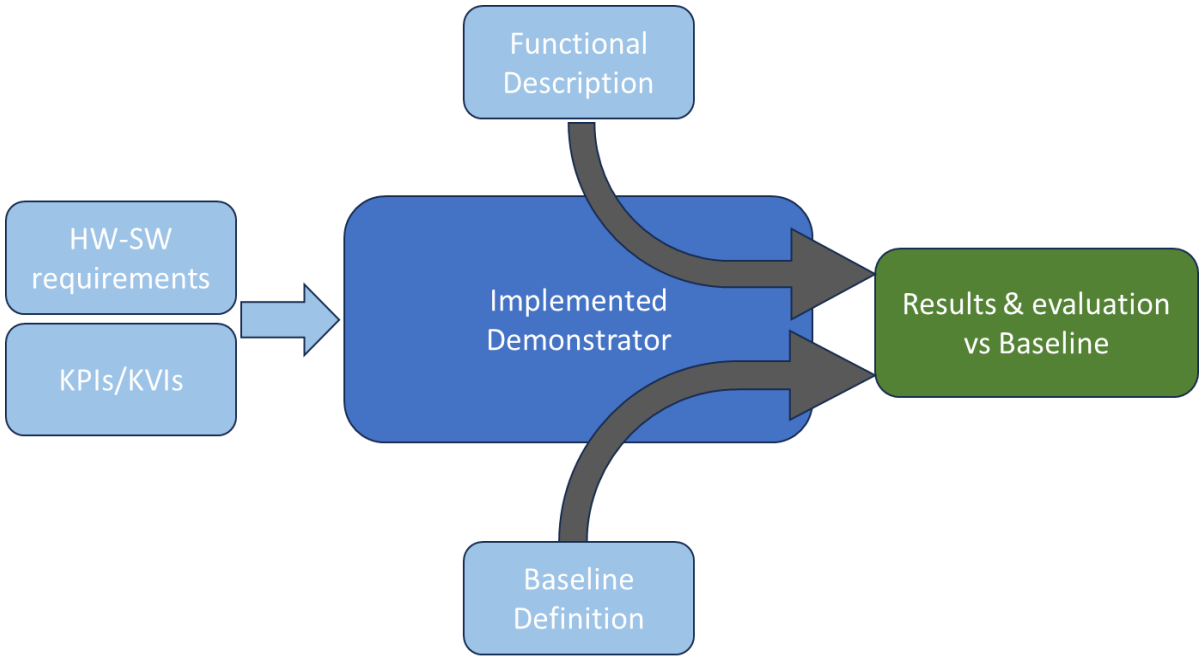

FIGURE 1. POC DEMONSTRATOR DEFINITION METHODOLOGY AND REQUIREMENTS.

Step 1. Describe the TC general design, coming from the work initiated in either WP2, WP3 or WP4 and try to ascertain what would be the most beneficial aspect of the TC for the end-user.

Step 2. If applicable, describe possible new functionality that the TC will bring versus the SoTA of the relevant research domain. If this functionality can be measured in some way, then specific KPIs will need to be defined in a later step. If the added functionality alone is a step beyond the SoTA, then a functionality validation operation procedure will need to be defined.

Step 3. The architecture of a demonstrator platform based on SW, HW or combination of the two will need to be defined. The way the envisioned TC will be integrated into the demonstrator platform, the foreseeing interface and the interactions between the TC under test and the demonstrator infrastructure will need to be clearly defined.

Step 4. Based on the presented architecture of the demonstrator platform, the SW/HW requirements of the demonstrator can be then defined and based on that, the feasibility of the demonstrator can be validated. We will need to make sure that the described demonstrators in this deliverable are feasible with the SW libraries/frameworks and the HW platforms available at the partners' premises. Any needed acquisition of extra HW and SW needs to be checked against the time framework of WP5 to avoid unavailability issues that could block the implementation of the PoC.

Step 5. If the proposed TC performance is quantitatively measurable, the proper KPIs/KVIs need to be defined or selected from the list of well-known KPIs/KVIs in the SoTA of the relevant research field, as well as the KPIs identified in WP2. Those KPIs and KVIs will be the main way of validating any performance or value gains from the adoption of the proposed TC.

Step 6. The KPIs defined in Step 5 should then be used to measure and define the general performance of a current SoTA system that will act as the baseline comparison against the offered performance of the relevant TC. This

comparison is of outmost importance, as it will clearly reveal any real advantages of the proposed new solution against the SoTA performance available today.

Step 7. Lastly, in this last step the demonstrator scenario should be clearly defined, meaning the exact steps with which the PoC will be put under test and the parameters that are going to drive the examination of the performance of the system. As an example, what type of network load is going to be enforced in a wireless transceiver in and what sequence? Which events are expected to happen in order to trigger some response? When will the measurement phase begin? Is there a transitional phase of the system we need to wait for to pass? Will we measure the selected KPIs in a stable state? Do we need to define events for start and stop of the measuring phase? etc. A clear definition of the demonstrator scenario will make the experiments easily reproducible and the results verifiable by third parties if needed.

Based on the above steps we have structured the presentation of each PoC in this deliverable to follow this logical sequence, taking of course into account the possible specific nature and context of the PoC.

3 PROOF OF CONCEPT ARCHITECTURE PRESENTATIONS

This section provides a presentation for each PoC architecture in terms of testbed that will be used, functionalities to be integrated and measurement of expected KPIs. The presentations below introduce the PoC testbed setup that is necessary to deliver each of the demonstrations.

3.1 LOW LATENCY CHANNEL EMULATOR

3.1.1 GENERAL DESCRIPTION

The wireless environment imposes many constraints and limitations on the performance of wireless telecommunication systems. Radio channel propagation characteristics, such as attenuation, shadowing, fast fading, variable delays, Doppler effect, noise, and interference cause severe degradation to all wireless transmission. Thus, the development of wireless communication systems requires rigorous testing to ensure that the products can operate even under the most demanding propagation environments. The traditional field-testing of wireless systems is generally labour-intensive, time-consuming, and expensive. Furthermore, even under the same test setups and test scenarios, the test results are typically non-repeatable since the propagation environment uncertainties plus external noise and interference affect the results. These factors necessitate radio channel emulation for enabling end-to-end full signalling performance validation and interoperability test in a laboratory environment, and hence become a standard way for the conformance testing of devices.

This PoC aims at a low-latency emulations of the channel models being developed in WP2, and that will be presented in deliverable D2.3, with expected submission in June 2024. The developed channel models will cover vehicular, industrial and consumer use case categories.

The PoC will leverage Keysight PROPSIM, a radio channel emulator that enables recreating the wireless channel propagation effects in a controlled laboratory environment. It is a one-box solution for performing a realistic and accurate emulation of all typical radio channel propagation effects such as multipath propagation, fast fading, dynamic delays, attenuation, noise, interference, and shadowing. The PROPSIM supports multiple channels, wide bandwidth, high dynamic range, and channel emulation with very high accuracy. The physical radio channel characteristics can all be emulated independently on PROPSIM supplementing, or even replacing traditional field-testing. PROPSIM product family is shown in Figure 2.

FIGURE 2. PROPSIM F64 F8800A (LEFT) AND PROPSIM FS16 F8820A (RIGHT).

The PROPSIM emulates only the radio channel excluding the transmitter and receiver characteristics and is thus independent of system technology. The PROPSIM supports all major wireless standards and signal types in a broad frequency range. It supports the development of the most demanding wireless applications, such as beamforming, massive MIMO, SDR, and aerospace satellite communications. In a typical test scenario, the transmitter and receiver to be tested are connected to the PROPSIM, which then emulates a wireless propagation environment, replacing the real radio channel, as illustrated in Figure 3. The PROPSIM uses real-world signals generated by external test equipment as an input.

The overall flexibility and extensive number of configuration options of the PROPSIM allow it to run several different types of tests and emulations. The emulations are based on preconfigured channel emulation files, stored in the PROPSIM. New emulation files can be added at any time by the users. The file-based emulation approach ensures full repeatability and controllability of the emulations. The PROPSIM includes pre-stored standard emulations (emulation connection diagram with channel models according to 3GPP). In basic use, the user only needs to load the emulation and adjust the power levels of the PROPSIM. For advanced use, all versatile channel modelling tools for creating user-defined channel models and modifying pre-defined standard channel models are available.

The PROPSIM includes an easy-to-use GUI that guarantees a quick emulation setup. The GUI can be used to control all aspects of the emulator functionality. It ensures that all emulation setup and configuration tasks require minimal manual work. The PROPSIM includes a “toolbox” of applications for creating channel models and emulations. Several channel models can also be combined for a single emulation which may use up to 128 fading channels, and thus up to 128 different channel models. The channel models are stored in the PROPSIM as pre-calculated files.

FIGURE 3. TYPICAL CHANNEL EMULATION TEST SETUP.

Under the scope of the 6G SHINE project, Keysight Technologies aims at improving the latency of its featured PROPSIM channel emulation platform to enable the emulation of short-range communication channel models for in-X subnetwork. As mentioned above, the low-latency channel emulations will be based on radio channel characterization and modelling framework for in-X subnetwork use cases identified in D2.1 of WP2/TC2. This work is currently in progress under Task 2.2a (radio channel measurements) and Task2.2b (radio channel characterization and modelling) of WP2. This is further elaborated in Subsection 3.5.7 where the scope of the demonstration scenario is discussed.

3.1.2 ENVISIONED ADDED/NEW FUNCTIONALITY

Low latency in the PROPSIM channel emulator can be achieved by optimizing the critical path for the radio signal inside it. The following key steps describe some latency optimization and implementation strategies that are being followed for reducing the latency of a critical path of the radio signal in PROPSIM.

1. The removal of unnecessary logic from the critical path could potentially shorten the signal path. This can be achieved by eliminating extra pipelining registers, as shown in Figure 4**Error! Reference source not found.**.

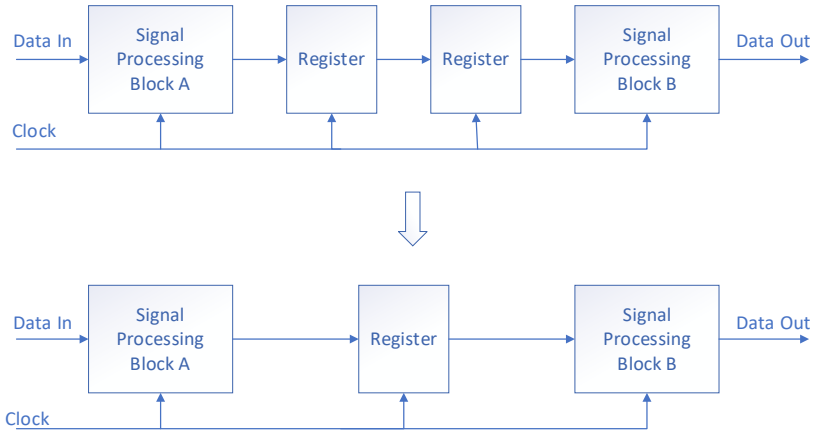

FIGURE 4. REMOVING UNNECESSARY LOGIC FROM THE CRITICAL PATH.

2. To further optimize the signal paths, the functional blocks can be combined. For instance, consecutive multipliers can be merged into a single multiplier component, as illustrated in Figure 5.

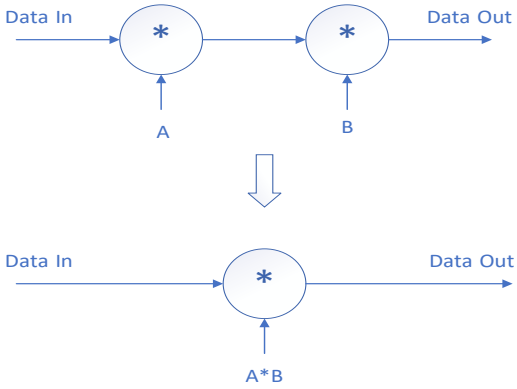

FIGURE 5. COMBINING FUNCTIONAL BLOCKS.

3. The rearrangement of functional blocks may allow to either combine them or further optimize their functionality which can affect the signal path latency, as depicted in Figure 6.

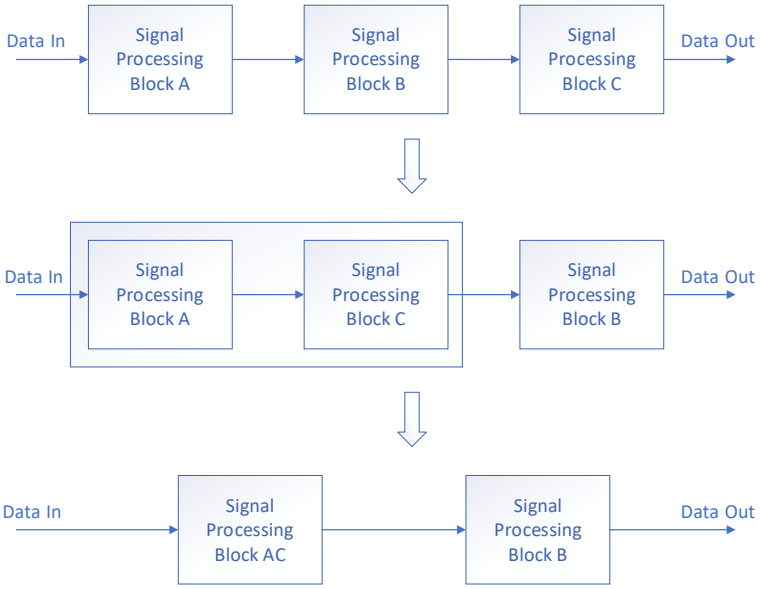

FIGURE 6. REARRANGING FUNCTIONAL BLOCKS TO AVOID REDUNDANCY.

4. The splitting of functional signal processing blocks and their subsequent parallelization into sub-blocks can also optimize the critical path signal path, as highlighted in Figure 7.

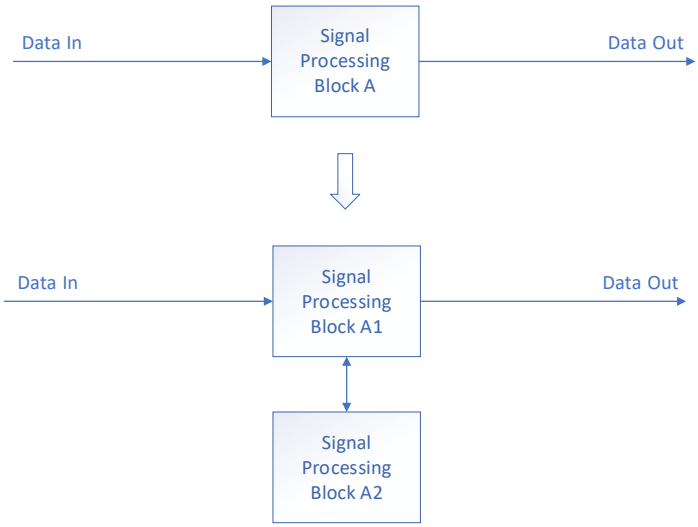

FIGURE 7. REDUCING COMPLEXITY BY SPLITTING SIGNAL PROCESSING BLOCKS.

5. The signal processing blocks (e.g. DDC/DUC filters) may also be optimized for latency.
6. Finally, the improvement in clock rate in different functional blocks may also help in improving the latency.

3.1.3 HW AND/OR SW REQUIREMENTS

3.1.3.1 KEYSIGHT PROSPSIM FS16

The PROPSIM FS16 channel emulator [1], illustrated through Figure 8, emulates the dynamic radio channels between transmitters and receivers in real time. The channel emulator supports uni- and bi-directional fading test configurations. The programmable multiport time and phase coherent PROPSIM RF transceiver platform provides full control of RF signal time, phase, and amplitude. In addition to real-time RF channel emulation, PROPSIM platforms support RF signal measurements and signal waveform transmissions with embedded signal analysers and waveform generators.

FIGURE 8. PROPSIM FS16 F8820A.

3.1.3.2 KEYSIGHT UXA SIGNAL ANALYZER

Keysight UXA signal analyser [2], shown in Figure 9, allow us to characterize the most challenging signals — fast-hopping, wideband, transient — in various wireless technologies, including 5G NR, Wi-Fi, satellite, radar, electronic warfare (EW), and more. Key features include.

- Analyse bandwidth-hungry emerging standards such as 5G and automotive radar with up to 1 GHz internal analysis bandwidth and up to 5 GHz external
- Make continuous sweeps up to 110 GHz
- Capture lower-level spurious signals with DANL as low as -150 dBm/Hz (> 50 GHz)
- Record and analyse real-world environments with gap-free streaming up to 255 MHz

FIGURE 9. KEYSIGHT UXA SIGNAL ANALYZER.

3.1.3.3 KEYSIGHT PNA-X NETWORK ANALYZER

Keysight's PNA-X [3], presented in Figure 10, is a vector network analyser and the most integrated and flexible microwave test engine for measuring amplifiers, mixers, frequency converters, and other active devices. The hardware includes two internal signal sources, a signal combiner, S-parameter and noise receivers, pulse modulators, and generators, and a flexible set of switches and RF access points. These hardware features provide a powerful core for a broad range of linear and nonlinear measurements, all with a single set of connections to the device under test.

- High source output power of +13 dBm at 1 GHz to +11 dBm at 67
- High dynamic range: 134 dB at 20 GHz at test port
- Low trace noise: 0.002 dB rms at 1 kHz bandwidth
- Low receiver noise floor
- High receiver compression level
- Fast measurement speed: 3.6 to 23 psec/point
- High stability: < 0.03 dB/°C

FIGURE 10. KEYSIGHT PNA-X NETWORK ANALYZER.

3.1.3.4 SOFTWARE

Each Keysight product has its own fully featured software suite to facilitate different RF measurement. The devices can also be interfaced and controlled through external programming scripts for automation. For measurements in

different validation setups that are explained in the preceding sections, Python/MATLAB based routines and apps are used for automating the measurements and data post-processing in the live setup.

3.1.4 HIGH LEVEL ARCHITECTURE OF THE ENVISIONED POC DEMONSTRATOR

The envisioned PoC for TC2 demonstration is conceived for the evaluation of key KPIs selected for the performance evaluation of the low-latency channel emulation platform, i.e., Keysight PROPSIM. The test bed is conveniently divided into two parts based on the testbed setups that can validate the set of KPIs and are discussed below.

3.1.4.1 PART1: INSERTION DELAY AND POWER DELAY PROFILE (PDP) VALIDATION

This first part of the PoC DEMO includes the validation of insertion delay and power-delay profile (PDP) to benchmark the performance of the PROPSIM channel emulator device in terms of low latency. For measuring the insertion delay of PROPSIM channel emulator, we follow the standard procedure for measuring the insertion delay of any device-under-test (DUT), which is described as follows. In general, a DUT may contain repeaters or other non-reciprocal elements that have a high loss in the return direction and prevent a reflection measurement. In cases where both ends of the link are available for measurement and a “through” measurement such as S21 is possible, a Vector Network Analyzer (VNA) can be a very effective tool for measuring electrical delay. The measurement setup for validating the insertion delay is shown in Figure 11.

FIGURE 11. MEASUREMENT SETUP FOR VALIDATING INSERTION DELAY AND POWER DELAY PROFILE (PDP).

In this method, a vector network analyser is used to measure the S21 of the DUT across a range of frequencies (S21 is the ratio of the voltage out of the DUT to the voltage in). A vector network analyser tracks phase as well as magnitude. For a device with a non-zero electrical delay, the phase shift between the input and the output of the DUT will change due to the frequency of the signal. Lower frequency signals have a longer wavelength than higher frequency signals and will go through fewer cycles passing through the DUT. Even for a perfectly linear DUT, the phase trace of S21 will have a slope that is related to the electrical delay.

By displaying the phase component of the S21 trace, we can observe the effect of the DUT on the signal at different frequencies and calculate the electrical delay. This is most easily done using an S21 trace, which is formatted in Figure 12 to show the “unwrapped” phase of the trace. The “wrapped” phase data “wraps” around so that the data does not exceed ±180 degrees. By showing the unwrapped phase, the network analyser displays the trace

data in a way that preserves long trends. A long increase or decrease in phase can be shown as passing through thousands of degrees.

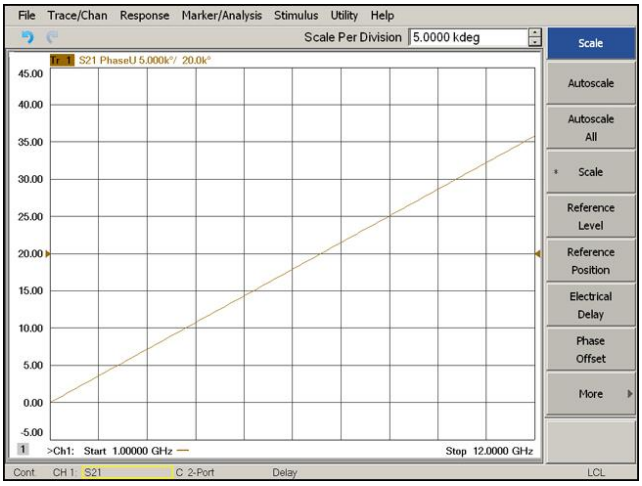

FIGURE 12. EXAMPLE UNWRAPPED PHASE TRACE OF DUT ELECTRICAL DELAY.

PDP measurements are also based on measuring S21 traces at VNA. For this purpose, the channel model defined according to WP2 Task2.2b will be loaded in the PROMPSIM emulator and the measured VNA traces, i.e., frequency responses $H(t,f)$, are saved into a hard drive. The data is read into software, e.g., MATLAB. The analysis is performed by taking the Fourier transform of each frequency response. The resulting impulse responses $h(t,f)$ are averaged in power over time. Finally, the resulting PDP is shifted in delay, such that the first tap is on delay zero.

$$P(\tau) = \frac{1}{T}\sum_{t=1}^{T}|h(t,\tau)|^2$$

The setup for measuring PDP is shown in Figure 11,while parameter settings for the measurements are tabulated in Table 2. The VNA transmits frequency sweep signals through the test system. Several traces (frequency responses) are measured and recorded by VNA and analysed by a post-processing SW, e.g., MATLAB. Special care must be considered to keep the fading conditions unchanged, i.e., frozen, during the short period of a single trace measurement. The fading may proceed only in between traces.

TABLE 2. VNA PARAMETERS SETTINGS.

Item	Unit	Value
Centre frequency	MHz	Channel model centre frequency
Span	MHz	200
Number of traces	MHz	1000
Number of points		1601
Averaging		10

3.1.4.2 PART2: DOPPLER SPECTRUM AND TEMPORAL CORRELATION VALIDATION

The second PoC DEMO part constitutes the measurement of the Doppler spectrum and temporal correlation of the in-X subnetwork channel emulation in PROPSIM. The Doppler spectrum is measured with a spectrum analyser according to the setup, as shown in Figure 13. In this case, a signal generator or VNA transmits a continuous wave (CW) signal to the PROPSIM which emulates it. Finally, the signal is analysed by a spectrum/signal analyser UXA, and the measured spectrum is compared to the target spectrum. This setup can be used to measure the Doppler

Spectrum of the channel models defined according to WP2 Task 2.2b. Sine wave (CW, carrier wave) signal is transmitted from the signal generator. The signal is connected from the signal generator to the fading emulator via cables.

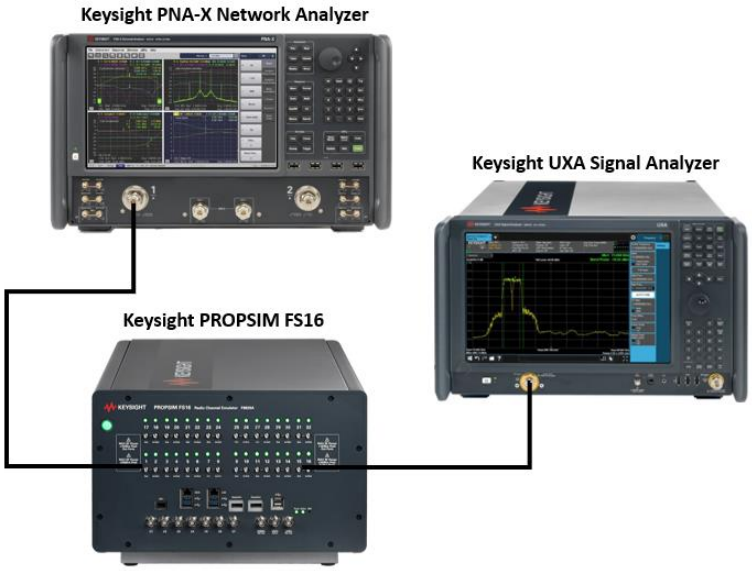

FIGURE 13. MEASUREMENT SETUP FOR VALIDATING DOPPLER SPECTRUM AND TEMPORAL CORRELATION.

The PROPSIM emulator output signal is connected to the Keysight UXA signal analyser, which measures the Doppler spectrum, and the trace is saved. The parameter settings of the UXA are tabulated in Table 3

The measurement data file (Doppler power spectrum) is saved into the hard drive. The data is read into, e.g., MATLAB. The analysis is performed by taking the Fourier transformation of the Doppler spectrum. The resulting temporal correlation function is normalized. Then the function values left from the maximum are cut out. Further on the function values after, e.g., seven periods are cut out.

TABLE 3. UXA PARAMETERS SETTINGS.

Item	Unit	Value
Centre frequency	MHz	Channel model centre frequency
Minimum Span	KHz	4
RBW	Hz	1
VBW	Hz	1
Number of points		160002
Averaging		100

3.1.5 APPLICABLE KPIS DEFINITION

For demonstrating TC2 through our PoC DEMO platform, following are the main KPIs that are crucial for the validation purposes. These will provide clear evidence if the PoC DEMO can provide expected results in terms of low latency. The measured and reference results will be compared quantitively for the validation of the KPIs.

3.1.5.1 INSERTION DELAY

The insertion delay refers to the time it takes for the RF signal at the input port to travel and reach the output port of the emulator device. In other words, it is the electrical delay that the emulator device adds to the overall latency.

3.1.5.2 POWER-DELAY PROFILE (PDP)

For wideband signals, the average received power as a function of delay is known as delay power spectral density, or popularly as power delay profile (PDP), describing the power decay of multipath as the time delay elapses. PDP

can be evaluated by taking the spatial average of magnitude squared channel impulse response over multiple observations in a local area or time. The example PDP is illustrated in Figure 14.

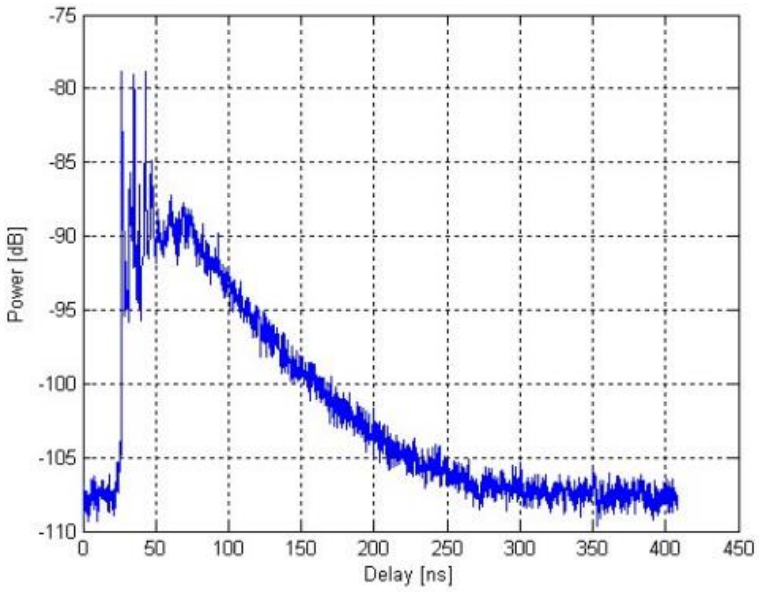

FIGURE 14. VALIDATION KPI: EXAMPLE POWER DELAY PROFILE (PDP).

3.1.5.3 DOPPLER SPECTRUM AND TEMPORAL CORRELATION FUNCTION

In a propagation environment, a signal propagates along multiple paths, such that the receiver experiences multiple time-delayed versions of the transmitted signal. Furthermore, if the user is moving, a Doppler spectrum arises, causing uncorrelated fading between the different received paths. An example Power Doppler Spectrum is shown in Figure 15.

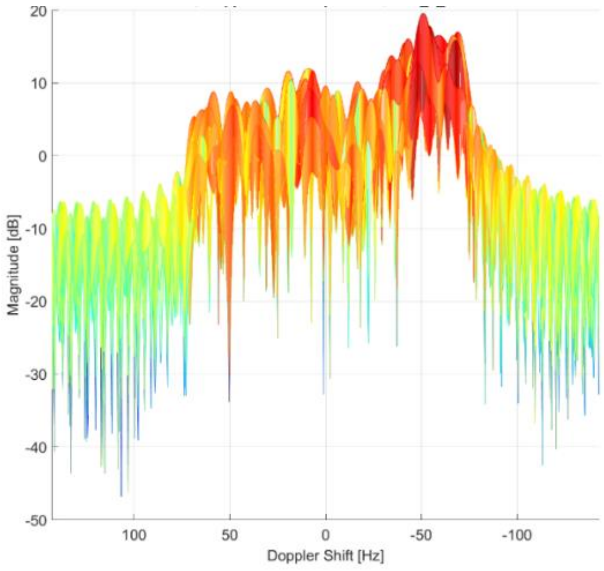

FIGURE 15. VALIDATION KPI: EXAMPLE POWER DOPPLER SPECTRUM.

The temporal autocorrelation function (TCF) describes how fast the channel changes in time. An example TCF is depicted in Figure 16.

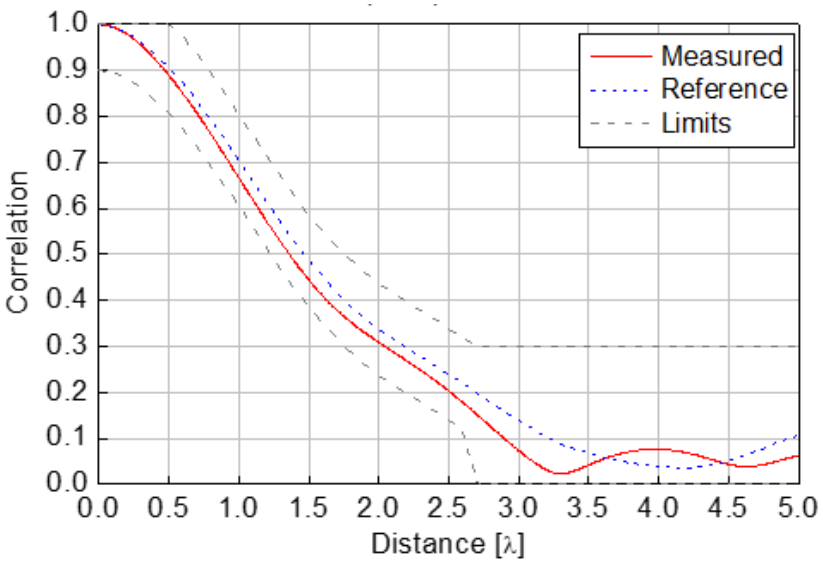

FIGURE 16. VALIDATION KPI: EXAMPLE TEMPORAL CORRELATION FUNCTION (TCF).

3.1.6 BASELINE DEFINITION

The current PROPSIM channel emulator platform offers an insertion delay of about 2.2 microseconds. The target low-latency PROPSIM platform aims at reducing the latency down to 1.2 microseconds in the initial PoC and up to 0.8 microseconds for the final PoC Demo. However, this is subject to the availability of hardware components and could delay the final implementation.

3.1.7 DEMONSTRATION SCENARIO

The low-latency channel emulations focusing on short-range communications are planned to be generated based on the channel models that will be developed based on the channel characterization and modelling effort in WP2 Task2.2a and Task2.2b. These channel models will be emulated at the radio frequency level and the emulation is interfaced with RF inputs and outputs. Key characteristics of channel models will be measured and demonstrated using RF test equipment, such as a network analyser or signal analyser. The key KPIs for the PROPSIM channel emulation test platform and channel model integration demonstration are the latency of the channel emulation measured through the insertion delay and the accuracy of the measured channel model characteristics, such as power delay profile (PDP), Doppler spectrum, and temporal correlation function (TCF). The usage of such an emulator allows reproducing harsh in-X propagation conditions which might be difficult to reproduce in laboratory facilities.

3.2 LATENCY AWARE MAC ACCESS

3.2.1 GENERAL DESCRIPTION

in-X subnetworks are expected to operate, among other possibilities, also in the unlicensed spectrum, where medium access policy limitation may hinder the possibility of achieving low latencies. In 6G-SHINE, solutions for improving latencies in the subnetworks operating over the unlicensed spectrum are studies.

The PoC architecture of the TC11 “Latency-aware access in the unlicensed spectrum” is here presented. The Latency Aware MAC scheme is focusing on providing wireless systems operating in the ISM bands with an enhanced access scheme that can offer true priority in high priority packets against the typical best effort approach as described by ETSI.

The core mechanism of the proposed scheme is based on a periodical non-contention-based period named LAD, that will have precedence against the basic CCA based access mechanism as defined by ETSI for ISM bands. The full details of this mechanism are described in deliverable D3.1. The PoC setup will focus to materialize a scenario of multiple nodes trying to service both best effort and priority flows, trying to acquire the medium in parallel. This will make possible the measurement of most important MAC and application layer KPIs related to the performance enhancement of priority flows as well as the possible deterioration of best effort traffic QoS. A comparison between the proposed scheme and the basic ETSI standard way of accessing the ISM bands will be made possible, in order to ascertain the pros and cons of the implementation of the proposed solution.

3.2.2 ENVISIONED ADDED/NEW FUNCTIONALITY

The Latency Aware MAC scheme will provide a new innovative enabler towards deterministic operation in a generic way, not focusing to any specific MAC design, but rather on the most general rules defined by ETSI for accessing the ISM bands. This will enable new MAC designs able to provide hard access priority in the medium for some packets when needed, in contrast with the traditional statistical properties-based priority differentiation that is used today in the most popular MAC protocols, like CSMA/CA or CSMA/CD. Packets having hard priority on the MAC scheme will have precedence in accessing the medium compared to other best effort traffic, significantly lowering their latency and the collision opportunity with best effort traffic.

3.2.3 HIGH LEVEL ARCHITECTURE OF THE ENVISIONED POC DEMONSTRATOR

The demonstrator will consist of 4 nodes that reside in the same wireless collision domain as depicted in Figure 17. Two of them will be running a legacy IEEE 802.11 MAC based on CSMA/CA following the current ETSI standard for accessing the ISM bands. The other two nodes will be running the proposed LA-MAC enhancement and will be sharing the medium with the legacy IEEE 802.11 nodes. As the proposed scheme will be an optional feature for any device wanting to enjoy hard priority access to the medium, it should be 100% transparent and able to coexist with the best effort service offered today. By transmitting best-effort traffic between the legacy nodes and priority traffic in the LA-MAC enhanced nodes, we will be able to measure the performance of both the best effort traffic flows as well as the priority flows to ascertain the performance of the proposed scheme as well as its impact on the best effort traffic.

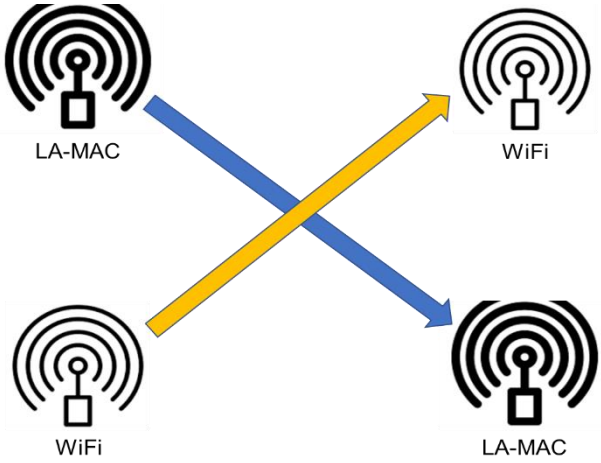

FIGURE 17. LATENCY AWARE MAC ACCESS POC DEMONSTRATOR.

All measurements will be stored in a database and possibly presented through a visualisation framework in real time. Hence, the demonstrator will be able to provide realistic results of the proposed MAC protocol performance and help to identify possible problems of implementation by comparing against the expected results based on the simulation studies executed in WP3.

3.2.4 HW AND/OR SW REQUIREMENTS

For this proof of concept, we will use the open Wi-Fi based IEEE 802.11 implementation for the legacy nodes, running on the zcu102 evaluation kit [4]. The radio frontend is provided by Analog Devices's FMCOMMS2 board [5]. For implementing the LA-MAC enhanced nodes we will use the same HW platform, replacing the CSMA/CA implementation with the LA-MAC version. Therefore, the demonstrator requires four ZCU102 development kits and four FMCOMMS2 radio frontends. All of them are available within IMEC's current HW portfolio.

3.2.5 APPLICABLE KPIS DEFINITION/PRESENTATION

For the performance evaluation of this PoC, we will use the KPIs presented below:

- Application layer:
  - Throughput, Latency, PSR.
    Measuring the end-to-end application layer throughput, latency and PSR will provide a clear picture of the user level performance and experience.
- MAC layer:
  - Medium access delay (average, min, max, standard deviation), PSR, jitter
    Medium access delay is the most important KPI for MAC performance, as it indicates the time a packet has to wait in MAC, before the medium access mechanism employed finds a spot for the packet to be transmitted. Of course, PSR must be taken also into account to make sure collisions do not occur when the packets are transmitted, else a low MAC delay is not indicative of correct and normal MAC operation (if for example 50% of the packets collide in the air, as it could happen with a simple ALOHA MAC, then a low MAC latency would be insignificant since 1 out of 2 packets does not make it to its destination).

3.2.6 BASELINE DEFINITION

To be able to evaluate the performance of the proposed mechanism, a baseline scenario based on the current SoTA MAC schemes in ISM bands needs to be set. To enable a fair comparison, we will use as baseline 4 nodes employing typical IEEE 802.11 (CSMA/CA) MAC protocol and try with the most current features supported for flow prioritisation to pass the same traffic as offered in the enhanced case. The baseline setup will be used to execute all scenario runs; therefore, a full picture of its performance regarding best effort but also priority traffic will be formed. In a next step, we will then compare the performance of this setup to the proposed new scheme, employing the relevant KPIs presented in the previous subsection. This will draw a clear picture of pros and cons of the proposed scheme against what is offered today for differentiated QoS services in ISM bands.

3.2.7 DEMONSTRATION SCENARIO

The demonstration scenario will follow the steps below:

1. The four nodes setup is initialized with the baseline CSMA/CA standardized MAC and a predefined application layer set of traffic flows will be pushed between the nodes, measuring relevant KPIs and thus forming the baseline of the setup for best effort and priority traffic.
2. Two of the nodes will then be upgraded to support the LA-MAC, and the same set of application layer traffic flows will be pushed on the nodes, measuring again the relevant KPIs.
3. A visualization tool will be used to plot the baseline vs the enhanced LA-MAC results, enabling the viewer to draw conclusions on the performance advantages and possible pitfalls of the proposed LA-MAC scheme.

3.3 JAMMING RESILIENT PHY

3.3.1 GENERAL DESCRIPTION

Jamming is identified as a critical threat to quality of services in the 6G subnetworks. In this PoC, we will demonstrate the baseband solution of a jammer resilient PHY. The proposed solution is based on the approximated log likelihood ratio (ALLR) based demapper, described in deliverable D3.1. In comparison to the typical SoTA threshold-based demappers, the ALLR based demapper takes into account interference and fading, and assigns appropriate confidence levels to the affected subcarriers, for the sake of improving performance. The PoC considers the case of a jammer interfering a communication link and aims at showing the performance benefit of the proposed solution with respect to a SoTA threshold-based demapper. Performance is analysed in terms of receiver sensitivity, packet error rate, throughput and latency in a given jamming or channel condition (i.e., the jammer's duty cycle, signal strength and spectral occupation).

3.3.2 ENVISIONED ADDED/NEW FUNCTIONALITY

This PoC is using the openwifi platform, and the ALLR based demapper on FPGA hardware is the key functionality added. Note that the channel estimation is an existing module in the platform, and it calculates channel state information to perform symbol equalization in an OFDM baseband receiver. This information is now reused by the ALLR based demapper to estimate the probability distribution of symbols, in order to calculate the likelihood ratios of the transmitted bits.

3.3.3 HIGH LEVEL ARCHITECTURE OF THE ENVISIONED POC DEMONSTRATOR

The PoC is established on top of open WIFI, which runs on a System on Chip (SoC) architecture. The SoC contains an ARM processor and a FPGA. Various high-speed connections are being used between the FPGA hardware and ARM processor, which is critical for a system requiring low latency real-time performance. On the ARM processor, an embedded Linux is running. Open WIFI then appears as a normal Wi-Fi card in Linux, and Linux provides necessary support for open WIFI from the higher layer. The overall architecture is shown in Figure 18.

We use the standard open WIFI FPGA image as the performance baseline, which still uses a SoTA threshold based demapper. In the first step, we measure the receiver sensitivity, which is the signal intensity at which the packet error rate is around 10%. Intuitively, the lower the receiver sensitivity, the better the performance. The receiver sensitivity measurement is done by connecting the CMW Wi-Fi tester with open WIFI board, and gradually lower its transmit power until a 10% packet error rate is reached.

Next, we run *iperf* or other user space tools (e.g., mgen, ping, etc) to measure latency and throughput, as well as packet error rate in a more sophisticated network setup. We use certain jamming condition, i.e. jammer's duty cycle, intensity and spectral occupancy is predefined, and measure the network throughput, packet error rate, and latency, and compare the performance of open WIFI with ALLR based demapper against the standard open WIFI FPGA image using the SoTA threshold-based demapper. We expect to see improved throughput and latency, and reduced packet error ratio.

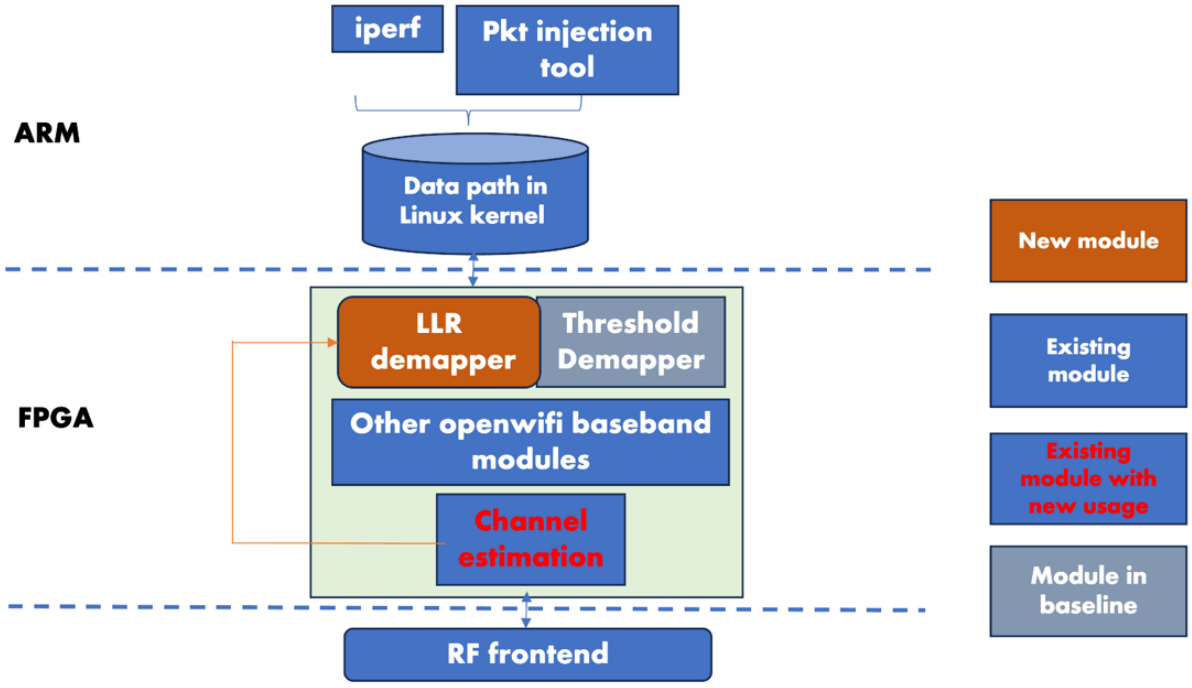

FIGURE 18. POC ARCHITECTURE OF JAMMER RESILIENT PHY ON OPENWIFI.

3.3.4 HW AND/OR SW REQUIREMENTS

For this proof of concept, we will use the open WIFI board that contains the most FPGA resources, which is the zcu102 evaluation kit [4]. The radio frontend is provided by Analog Devices's FMCOMMS2 board. In addition, the receiver sensitivity test requires the use of R&S CMW 270 wireless connectivity tester [6]. In order to create the interference scenario, we plan to use the USRP software defined radio, as well as several commercial off-the-shelf devices, such as Zigbee Zolertia Re-mote [7], which are all available in the IMEC wilabt testbed [8].

3.3.5 APPLICABLE KPIS DEFINITION/PRESENTATION

In this PoC experiment, we will use the following metric as KPIs:

- Receiver sensitivity: we measure the receiver sensitivity, defined as the signal intensity at which the packet error rate is around 10%, with and without the jammer resilient feature.
- Packet error rate: we measure the packet error rate at physical layer, defined as the ratio of packet failed to be decoded against the total transmitted packets, with and without the jammer resilient feature, under the same interference scenario.
- Throughput: we measure the amount of bit transferred in a given time unit between devices, when the jammer resilient feature is first disabled and then enabled, under the same interference scenario.
- Latency: we measure on average the time it takes from when a packet is prepared in the sender's application layer till it arrives at the receiver's application layer, with and without the jammer resilient feature, under the same interference scenario.

3.3.6 BASELINE DEFINITION

The default open WIFI PHY performance is our baseline. The default open WIFI PHY is using 64 sub carriers in an OFDM symbol, on each subcarrier BPSK, QPSK, 16 QAM and 64QAM can be applied with several coding rate on the convolutional encoder. The demapping in the default open WIFI image implementing the SoTA threshold-based

demapper is achieved by comparing a symbol's I and Q component against predefined thresholds. This is our baseline to show the advantage of the proposed concept.

3.3.7 DEMONSTRATION SCENARIO

The demonstration will be executed in the following steps:

1. A link formed by two SDR boards will be established, with the default FPGA image (without the ALLR demapper feature).
2. Jamming network will also be established, with the required duty cycle and strength.
3. We measure the physical layer performance of the link formed by two SDRs with the relevant KPI.
4. We will upgrade the SDR boards with the FPGA image enabled with the ALLR feature and measure the same KPI under the same jamming condition.

3.4 INTRA-SUBNETWORK MACRO-DIVERSITY

3.4.1 GENERAL DESCRIPTION

In spite of the short-range communication, the possibility of achieving ultra-reliable low latency communication in in-X subnetworks might be hindered by blockage and obstructions. Intra-subnetwork macro-diversity solutions are currently studied in WP3 for the sake of strengthening reliability by providing redundant robust radio links. This PoC aims at demonstrating the network coded cooperation concept for in-X subnetworks presented in deliverable D3.1.

Network coded cooperation relies on the overhearing capabilities of the devices, i.e. devices may overhear packets for other recipients, and use this information for re-encoding the packets. In this PoC, data packets are coded with each other at the symbol level, based on arithmetic in finite fields. Packets can then be transmitted either in their native form, or in a combined form. Leveraging the combination of combined and native packets at the receiver side is known to enhance performance robustness. We expect that the introduction of network coding has a huge influence on latency and reliability in wireless communication and will be a significant improvement compared with retransmission schemes.

The PoC is based on UWIN, an industrial radio system developed by Fraunhofer IIS. UWIN is a wireless communication system which aims to replace or extend traditional wired field buses in industrial automation applications. In order to support closed loop motion control over radio, UWIN has a low latency and maintains cycle times as low as 125 µs.

In the PoC, a network of UWIN nodes will be first configured for traditional single link operations, and performance will be evaluated. Then, the experiment will run again enabling the network coded cooperation scheme, for the sake of highlighting its benefits.

3.4.2 ENVISIONED ADDED/NEW FUNCTIONALITY

The communication system in our PoC consists of one base station and multiple field devices (see Figure 19). The hardware is based on a software defined radio platform which is controlled by an FPGA for maximum performance.

Two radio systems will communicate simultaneously on two physical channels. This allows for a higher channel capacity which can be used for either a higher throughput or more reliability.

FIGURE 19. UWIN SETUP WITH ONE BASE STATION AND TWO FIELD DEVICES OF THE WIRELESS COMMUNICATION SYSTEM.

The current network is implemented in a star topology. This allows for a simple centralized data flow but limits the throughput between the nodes since all traffic is routed through the base station. The current system also ignores data from the side links which could be used to further improve the reliability.

In 6G-SHINE the communication system will take advantage of the side links by introducing the network coded cooperation scheme to the wireless communication. A real-time processor in the data path allows for simple modification and extension of the coding scheme. This way multiple network coding concepts and implementations can be validated and compared.

While the base station has a dual RF tuner for simultaneous transmission on two channels, the current field devices are equipped with a single tuner. In 6G-SHINE every node will be equipped with a dual tuner. This allows for network coding via two parallel channels.

3.4.3 HIGH LEVEL ARCHITECTURE OF THE ENVISIONED POC DEMONSTRATOR

The overall architecture of our PoC is depicted in Figure 20. The RF tuner and the RF frontend are controlled by the FPGA. The FPGA firmware takes care of all timing critical tasks such as synchronization and scheduling. The data is transferred from the FPGA to the real-time ARM core whose software processes the real-time data, performs coding and decoding and bridges the data to the wired field bus. Management and control tasks which are not real-time critical are performed on the application core.

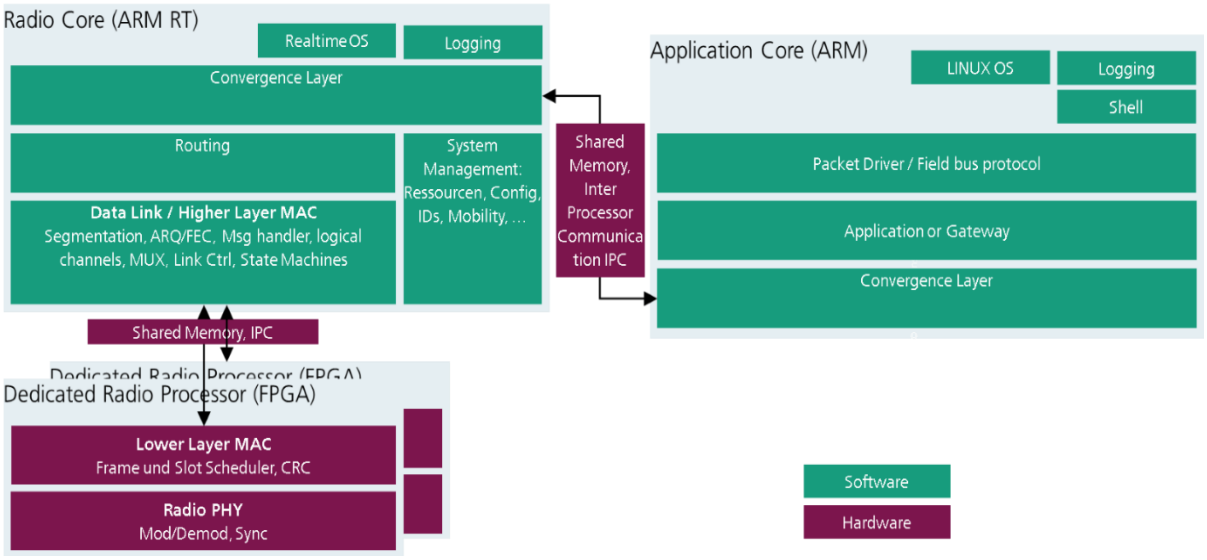

FIGURE 20. SYSTEM ARCHITECTURE OF THE UWIN WIRELESS NODES.

3.4.4 HW AND/OR SW REQUIREMENTS

The hardware consists of an FPGA board, an RF tuner module and an RF frontend. The FPGA is coupled with multiple ARM processors. One application ARM core runs Linux, one real-time ARM core executes communication tasks on an embedded real-time operating system.

3.4.5 APPLICABLE KPIS DEFINITION/PRESENTATION

The main KPIs of the developed UWIN-based system are the following:

- Telegram loss rate, defined as the mean number of lost telegrams per transmitted telegrams. A telegram is lost when it cannot be decoded at the receiver and the forward error correction cannot correct it and all its retransmissions are lost.
- Cycle time, defined as the time in which every node sends and receives its data for one cycle.
- Number of nodes to be served within the cycle time. The cycle time is fixed for a given number of nodes.

The thee KPIs influence each other. For example, the introduction of retransmissions lowers the telegram loss rate but leads to an increased cycle time or a lower number of nodes.

3.4.6 BASELINE DEFINITION

The KPIs of the current UWIN system is the baseline for our proof of concept. In the current implementation (i.e., without network coding), the scenario with the lowest latency offers a telegram loss rate of 10^{-7} at a cycle time of 125 µs with 4 field devices. The scenario with the highest number of nodes offers a telegram loss rate of 10^{-7} at a cycle time of 1 ms with 100 field devices. We aim at improving upon these requirements by exploiting network coded cooperation.

3.4.7 DEMONSTRATION SCENARIO

The demonstration will be executed in the following steps:

1. A network of UWIN nodes is configured with the baseline configuration without network coding.

2. A long-term laboratory test is performed in order to record the baseline performance.
3. The network is configured with a network coded cooperation scheme.
4. The long-term test is repeated in order to verify that the performance has improved.

3.5 CENTRALIZED RRM

3.5.1 GENERAL DESCRIPTION

Centralized radio resource management relies on the capabilities of a parent network of coordinating the radio resources of the in-X subnetworks in its coverage area. This PoC addresses centralized interference management in dense subnetwork deployments, with reference to in-vehicle use cases. Centralized radio resource management is currently being studied in WP4, and initial results will be presented in Deliverable D4.1, to be submitted in June 2024.

The PoC aims at establishing a wireless connected Electric-Electronic (E/E) architecture. As a first step, we plan to build a detailed vehicle communication infrastructure to demonstrate autonomous driving (AD) applications, such as road sign detection. Parts of the E/E architecture components are integrated, pre-processed and transmission happens through a wireless communication environment, potentially using Wi-Fi COTS components. The next step is to centrally manage the interference between multiple vehicles by enabling a parent-network triggered subnetwork configuration. This approach allows us to incorporate context information, such as the position and heading of subnetworks, to perform proactive resource allocation.

3.5.2 ENVISIONED ADDED/NEW FUNCTIONALITY

We aim at implementing the following functionalities:

- Implementation of subnetwork controller and subnetwork element within a vehicle E/E architecture.
- Implement gateway functionality in subnetwork controller including local/external routing.
- Protocol tunnelling or native support over subnetwork for user data transport.
- Implement subnetwork management control function baseline as distributed function between subnetwork controller and parent network.
- Establish control channel and basic APIs that enable key functions such as discovery, registration, state machine, which handles the connected states of subnetworks.
- Enable parent-network triggered subnetwork configuration based on connected state.
- Implement a higher-layer controlled centralized RRM by the parent network.

3.5.3 HIGH LEVEL ARCHITECTURE OF THE ENVISIONED POC DEMONSTRATOR

The PoC is established by initially building a vehicle communication infrastructure where components of the E/E architecture can be simulated and emulated following the concept of Hardware-in-the-loop (HIL) and Software-in-the-Loop (SIL) [9]. More specifically, components of the E/E architecture, in this case automotive cameras, act as the interface between the plant simulation and the embedded system under test, allowing us to establish wireless connections between these components. The general view of the PoC is represented in Figure 21, while details of the communication infrastructure, which is the main purpose of this PoC, can be seen in Figure 22. A subnetwork controller entity is responsible for managing the wireless connectivity between the elements within the in-vehicle subnetwork. This controller is connected to a vehicle central connectivity unity (CCU) through a Switch, which serves as a communication interface between the subnetwork controller and a parent network. The parent network is responsible for radio resource management between adjacent subnetworks. The subnetwork controller entity can receive monitoring data from each subnetwork and send commands to the subnetwork controller to manage interference.

We expect to see AD applications, i.e., road sign detection, being enabled through the wireless communication infrastructure. This means, for example, that the connection between the automotive camera and the zone Electric control unit (ECU) is wireless. Additionally, we must keep monitoring interference level against potential adjacent networks, and, based on network policies, triggering radio resource management actions, a concept illustrated in Figure 23. On top of that, to enable such services, we have also to develop layers of security, safety, and data conversion.

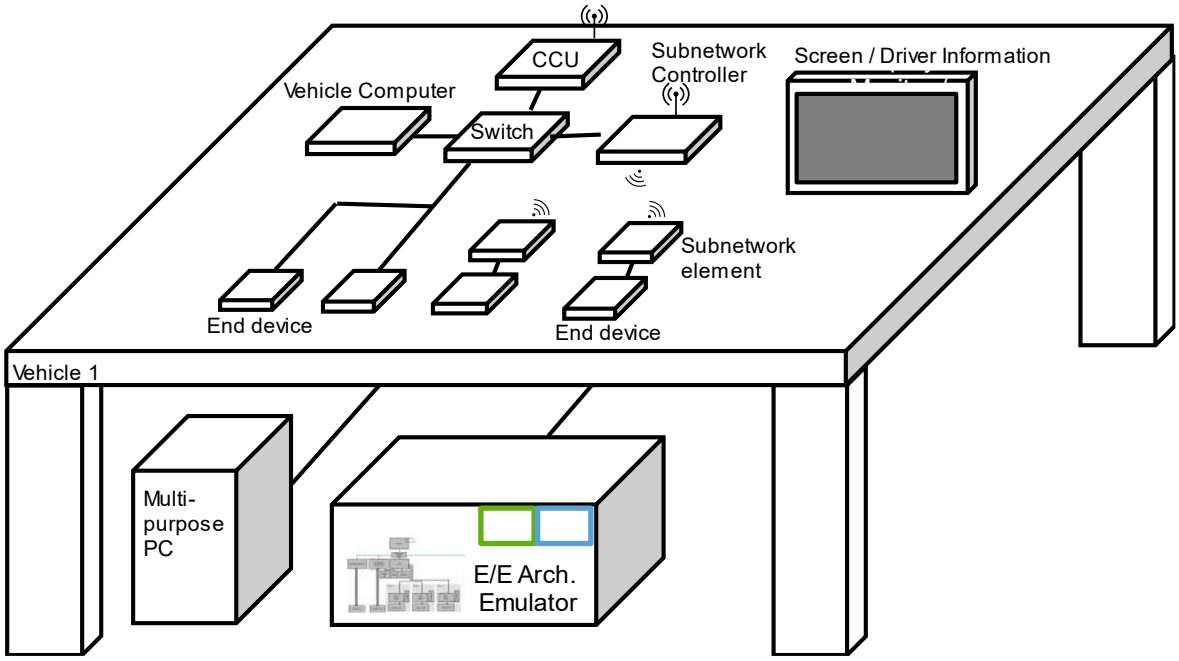

FIGURE 21. GENERAL OVERVIEW OF THE PLANNED POC.

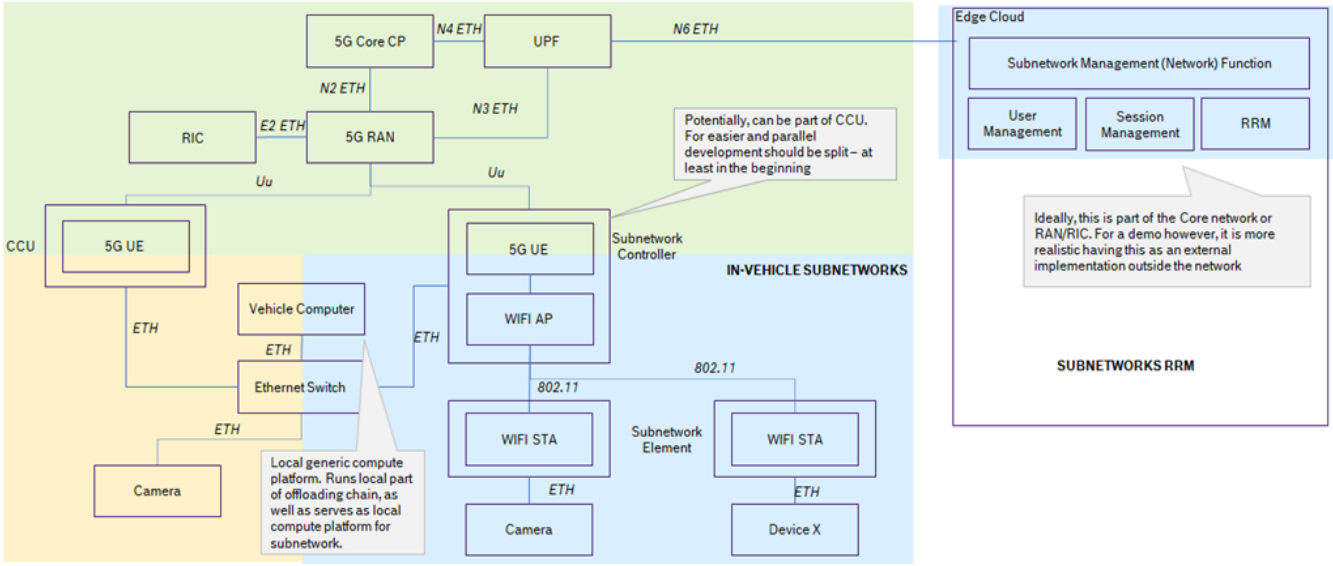

FIGURE 22. MAIN BUILDING BLOCKS ENABLING THE POC DEVELOPMENT.

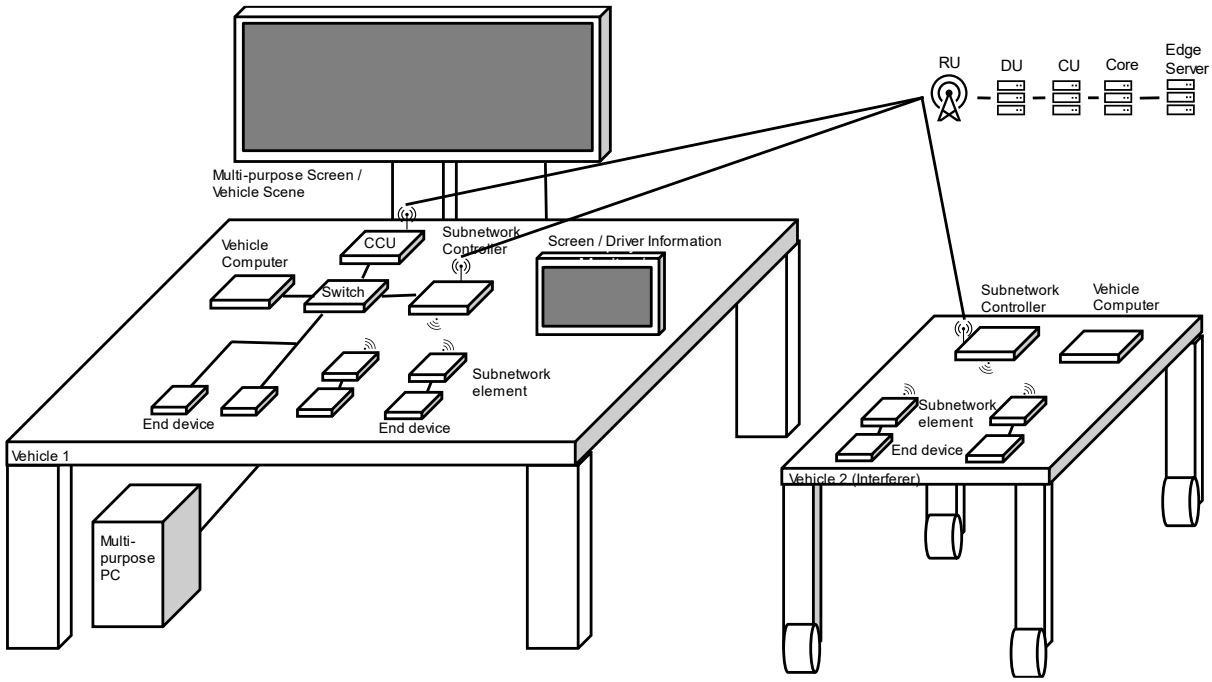

FIGURE 23. CENTRAL RADIO RESOURCE MANAGEMENT BETWEEN IN-VEHICLE NETWORKS.

3.5.4 HW AND/OR SW REQUIREMENTS

The following hardware will be used in the PoC: Local Vehicle Compute Node (e.g., Raspberry pi), automotive camera for ADAS, connectivity control unit (CCU), Smart Radar (only object list), or raw Radar with pre-processed data (100MBit/s).

We will be operating with Linux OS, and use the Open WIFI/OpenWRT driver.

3.5.5 APPLICABLE KPIS DEFINITION/PRESENTATION

For the evaluation of the wireless performance, Packet Error Rates, SINR (Signal to Interference plus Noise Ratio) values, and the end-to-end latency of the network between certain components are planned to be measured. In addition, it is planned to analyse, whether and how much the wireless links influence the performance of the application. To this end, application specific KPIs will be considered, such as object detection accuracy.

3.5.6 BASELINE DEFINITION

Our current baseline relies on the wired connectivity of E/E architecture components. Our goal is to achieve similar performance using wireless communication devices, while also adding layers of security and Radio Resource Management.

3.5.7 DEMONSTRATION SCENARIO

The scenario is envisioned to be modelled as depicted in Figure 3. An automotive camera, connected to a vehicle computer via a commercial off-the-shelf Wi-Fi device, is performing a road sign detection task. However, when an adjacent vehicle approaches as an interfering agent, the image quality is directly affected, thereby impacting the automotive service, which is displayed on the driver information screen. By implementing our central sub-network

solution, we can achieve two key objectives: 1) predict when the interference is likely to occur and 2) take appropriate actions to mitigate its effects.

3.6 CENTRALIZED/DISTRIBUTED INTERFERENCE MANAGEMENT

3.6.1 GENERAL DESCRIPTION

Besides centralized radio resource management, where radio resources such a spectrum and power, are managed by the in-X subnetworks, distributed and centralized radio resource management techniques are also of interest in 6G-SHINE. When distributed radio resource management techniques are used, subnetworks are capable of autonomously perform their decision, based on e.g., local learning or information exchange with neighbours' subnetworks. Such solutions are currently studied in WP4, and initial results will be presented in deliverable D4.1, with expected submission in June 2024.

This PoC is meant to address both centralized and distributed radio resource management solutions, relying on deep learning (DL) methods. In particular, the centralized solution is meant at enabling a central node to learn the transmission mode of different devices for the sake of optimizing resource scheduling while in the distributed solution, subnetworks will autonomously optimize the transmit power based on the perceived interference level from neighbour subnetworks.

3.6.2 ENVISIONED ADDED/NEW FUNCTIONALITY

This PoC consists of 2 in-X subnetworks with 2 served devices, and will be integrated into srsRAN, an open source 5G protocol stack [10], that will be tested in advance for a single cell scenario and expanded to two cells use case.

The following two application scenarios will be demonstrated:

- Centralized coordinated resource management, assuming devices with different traffic requirements, i.e., periodically scheduled devices via configured grant (CG), and dynamically scheduled devices. Deep reinforcement learning (DRL) methods will be used at a central node to learn the transmission patterns of these devices. Such information will be used to manage scheduling resources between periodic and dynamically scheduled devices for the sake of minimizing interference.
- Distributed resource management for the same type of devices. In this case, the DRL solutions will be running in both subnetworks and each subnetwork will be able to learn about the interference power and pattern of the neighbour. This will enable the possibility of managing autonomously the power allocation in subnetworks, leading to a distributed power allocation solution.

3.6.3 HIGH LEVEL ARCHITECTURE OF THE ENVISIONED POC DEMONSTRATOR

The PoC will rely on URLLC 3GPP Release 17 features, such as CG, that will be implemented and integrated into the srsRAN platform. A depiction of the principle of our centralised/distributed interference management is shown in Figure 24. We adopt the nomenclature defined in WP2 with respect to the roles of subnetworks nodes; in particular, high capability (HC) devices as the devices able to perform scheduling decisions, and subnetwork elements (SNEs) as the served devices. Based on the AI/ML methods running in the HC node, either distributed or centralised interference management solutions will be provided for CG and CG/dynamic devices as well.

In the former, the HC will learn by themselves about their CG based users, while for the latter a coordination will take place for the additional CG users. An HC node will be able to control its power under a certain distributed power control framework that will rely on message-passing neural networks (MPNN). The MPNN normally requires extensive feedback for each neural network layer execution. However, in order to reduce the signalling overhead for message-passing, an over the air MPNN (Air-MPNN) approach can be used as proposed in [11]. Since the received power of the pilot signals on the interference links depends also on the channel state information (CSI)

of the interference links, the CSI is included with the message passing information (MPI) to reduce the signalling overhead.

Such an Air-MPNN framework enables each node to select the transmit power according to its local features and local embedding during the message passing and aggregation phases. After that, all the nodes broadcast their pilots simultaneously. The considered Air-MPNN framework only requires all the nodes to broadcast the pilot simultaneously without extra CSI among the other nodes. This reduces the feedback significantly while the interference management does not downgrade their performance. Details about the solution will be presented in deliverable D4.1 by considering different deep neural networks that will result in centralized and distributed solutions. Notably, the Air-MPRNN method can be potentially integrated into the existing wireless networks such as 5G NR and WiFi without changing their frame structures. To this end, our PoC could also leverage the Open WIFI stack (i.e. one pair of HC/SNE could be deployed with Open WIFI while the other with the srsRAN) using the Zynq platforms to deploy the proposed in-X solutions for both systems.

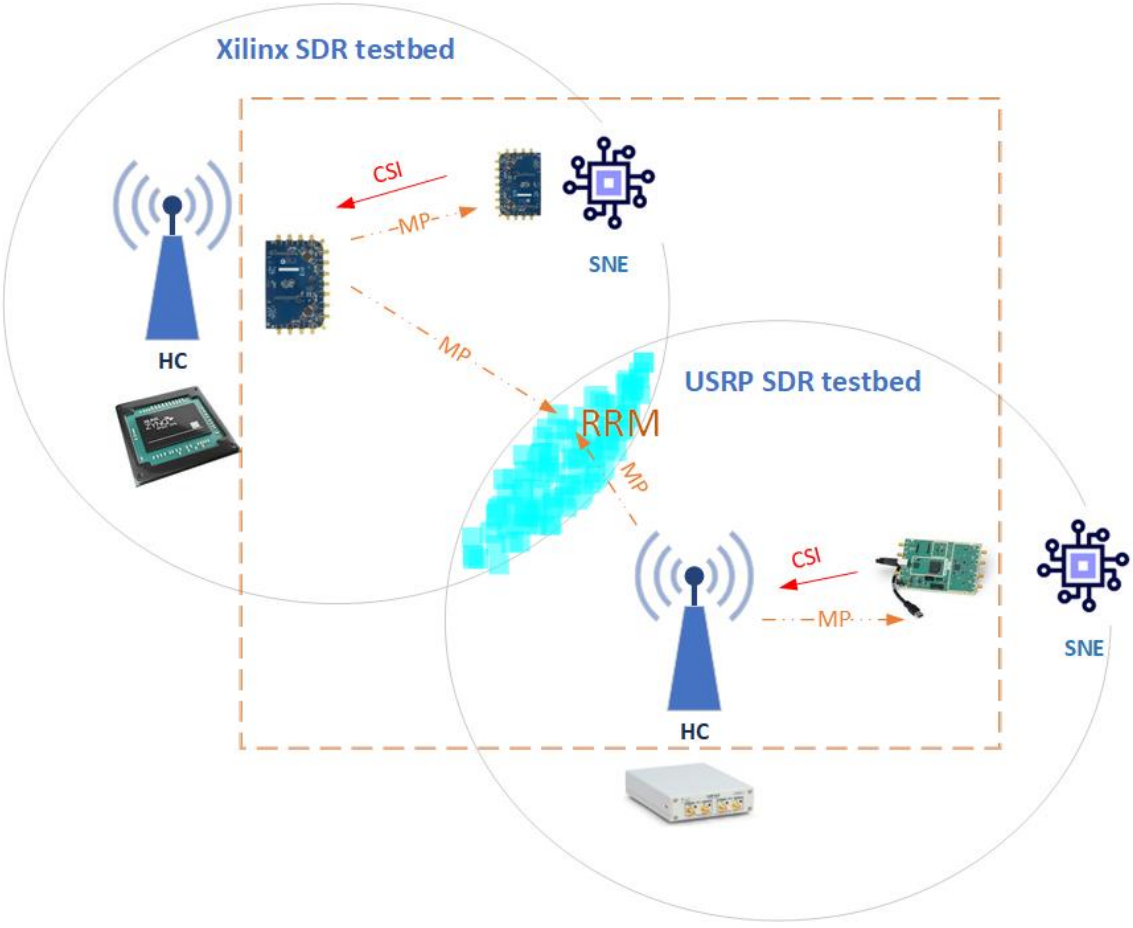

FIGURE 24. POC SETUP FOR THE CENTRALIZED/DISTRIBUTED INTERFERENCE MANAGEMENT.

3.6.4 HW AND/OR SW REQUIREMENTS

The PoC will use two AMD FPGAs from Zynq 7000 SoC family, one ZC702 and one ZC706 [12]. Both FPGAs allow connection with external development cards through Dual FPGA Mezzanine Card (FMC) Interface. Using this interface, two AD-FMCOMMS5-EBZ SDR cards, from Analog Devices, are connected on each FPGA [12]. These cards host two AD9361 transceivers, each one of them with dual transmitters and dual receivers, supporting in total 4x4 MIMO configuration. The supported working central frequency starts from 70MHz up to 6GHz, while the supported bandwidth is in range 200KHz to 56MHz, suitable for prototyping and developing wireless communication applications. These applications can be hosted on the ARM Cortex embedded processor, which is incorporated on each FPGA, utilizing the transceivers using LibIIO drivers, or from external hosted machine through the Gigabit

Ethernet connection. There are also two USRP B210 SDR kits, which incorporate an AMD Spartan 6 FPGA and also an AD9361 transceiver. This kit does not have an embedded processor and thus all applications are hosted on external machine, which is connected through fast SuperSpeed USB 3.0, using Universal Hardware Drivers (UHD). The spectrum band that will be used for the demo will be decided according to the best possible application scenario.

3.6.5 APPLICABLE KPIS DEFINITION/PRESENTATION

In this PoC, we will use the following metrics as KPIs that are relevant to latency and reliability as well:

- Packet error rate (PER): we measure the packet error rate at physical layer, defined as the ratio of packet failed to be decoded against the total number of transmitted packets.
- Throughput: we measure the average amount of transferred information in a defined period between devices, and in the subnetwork.
- Latency: we measure on average the time it takes when a packet is prepared in the sender's application layer till it arrives at the receiver's application layer.

Any other relevant to the testbed platform KPI will be listed in deliverable D5.2, where we will have already first testbed results available.

3.6.6 BASELINE DEFINITION

The baseline scheme considers subnetworks not to be equipped with radio resource management capabilities. This means, the subnetwork can perform their power allocations autonomously without any centralized or distributed joint decisions to enhance the performance of the in-X subnetworks by reducing the introduced interference.

3.6.7 DEMONSTRATION SCENARIO

The demonstration scenario will have the following structure:

- Two HCs will work in the same spectrum band and serve their associated SNE. Two SNE will be considered for the PoC, considering the setup with 2 Xilinx+AD and 2 USRP SDR boards.
- In the connection setup, the 2 Xilinx+AD will play the role of one HC/SNE pair and the 2 USRPs will play the role of the second HC/SNE pair. Different setups might be also possible in order to facilitate the communication between the 2 HCs.
- The 2 HC nodes will interfere each other due to the close distance between them and using the same band. This will be tested in a lab environment.
- The 2 HC boards will provide deep learning-based interference learning capabilities. The message passing solution will be implemented through the srsRAN (and possible open WIFI as well) deployed on the boards for the CG and dynamic scheduling users.
- The centralized and distributed interference management will take place among the two HC boards through a communication interface such as Ethernet.

3.7 JAMMING DETECTION USING ANOMALY DETECTION METHODS

3.7.1 GENERAL DESCRIPTION

As mentioned in section 3.2, jamming is a significant threat to critical services in subnetworks. While the PoC presented in section 3.2 focuses on detector enhancements, this PoC demonstrates a framework where anomaly

detection methods for jamming detection are implemented at the radio access level of a subnetwork and used as inputs for traffic management methods in the 'umbrella' network, (e.g., switching to different edge nodes for serving the subnetwork traffic). The corresponding methods are currently being studied in WP4 and will be included in the coming D4.1 deliverable, expected by June 2024.

In this PoC, we will collect or model different measurements (e.g., latency, packet error rate, etc.) with and without jammers in the radio access and use these measurements to develop/train an anomaly detection unit (e.g., autoencoder). This will allow us to use the unit for jammer detection and also to understand the level of interference caused by the jammer and its impact on network performance. This information will be used as an input into the 'umbrella' parent network, which in our PoC will be represented by the internally developed platform AdventEdge.

The platform will allow us to model functionalities of the parent network, for example switching users from subnetwork affected by jammer to neighbouring overlapping subnetwork not affected by the jammer and hence switching between edge nodes in order to serve the traffic. We may consider different scenarios such as: 1) Scope within a subnetwork and 2) Scope between subnetworks. In the first case, the anomaly detection unit may reside at the HC level and perform scanning of the RF environment (periodically or configured) and use these measurements to potentially detect jammers based on trained algorithms. The second case, the anomaly detection unit may reside at gateway level, will have higher complexity, and use measurements from several subnetworks in order to potentially detect jamming events. For the PoC, we will start with the simpler case and focus within a level of subnetwork. It should be noted that for the training stage of the anomaly detection unit we will use different inputs such as based on measurements, traffic profiles, or by following certain model distributions.

3.7.2 ENVISIONED ADDED/NEW FUNCTIONALITY

The added functionality will be two-fold: 1) Design of an anomaly detection unit with the capability to detect jammers within subnetworks, and 2) Mechanism that uses the information about the detected jammer as input to enable traffic management functionalities in the 'umbrella' network, such as switching between different computation or traffic serving nodes. It should be noted that the novelty of the proposed functionality may be subject to change and modifications as the research conducted in WP4 progresses. One example of autoencoder including the main blocks and objective function that may be used in the implementation is depicted in Figure 25. The algorithm will be implemented in Python, similarly to the integration with the AdventEdge. The AdventEdge may run on a dedicated NUC unit.

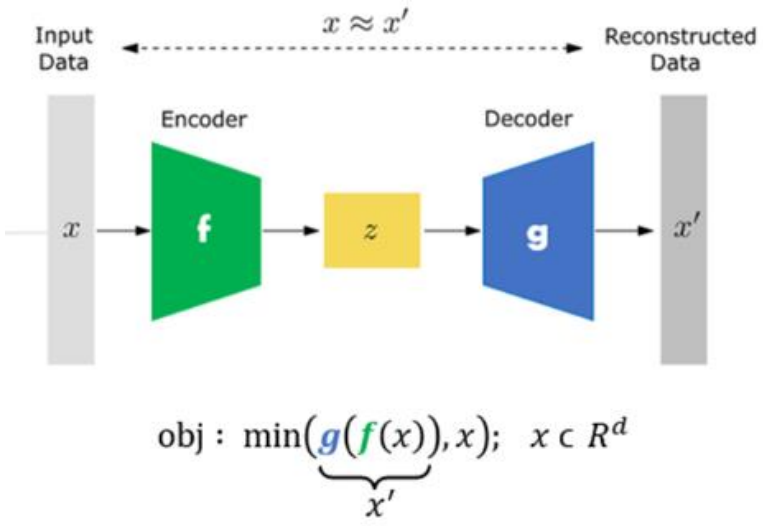

FIGURE 25. ILLUSTRATION OF AUTOENCODER USING MAIN BLOCKS AND OBJECTIVE FUNCTION.

3.7.3 HIGH LEVEL ARCHITECTURE OF THE ENVISIONED POC DEMONSTRATOR

The high-level architecture of the demonstrator is depicted in Figure 26. In the left-hand side dashed square, the entities related to the radio access of the subnetwork are shown. These include users, HCs devices and a potential jammer. In the right-hand side dashed square, there entities related to 'umbrella' network are captured such as compute nodes. A 6G base station entity connects the two sides of the architecture. The anomaly detection algorithm will be deployed at the level of HC devices using the data collected by these nodes (or alternatively it may have a BS level implementation), whereas the switching logic will be deployed at the 'umbrella' network and will involve switching between different compute nodes. It should be noted that the functionality of the entities in the architecture adheres to the definitions derived in WP2, as listed below:

- **Subnetwork elements:** are computationally constrained devices that have limited form factor, cost footprint, and include devices such as sensors/actuators. A SNE device can be a user equipment as defined by 3GPP or a non-3GPP device.
- **High capability (HC)**: Element with High Capabilities, an element with high capabilities is a device/node with increased capabilities in terms of networking and computation. Such a node might act as the central communication node in a subnetwork and might offer compute resources to other devices in the subnetwork. Multiple such HCs can be installed in a single subnetwork. An HC device can be a user equipment as defined by 3GPP or a non-3GPP device.
- **6G base station (6G BS):** A 6G base station comprises the radio access network components of the parent network, to which subnetworks can be connected. It might realise a subset of the signal processing and coordination functionalities under investigation in WP3 and WP4.
- **Compute node (CompN)**: 6G network compute node A 6G compute node is a component that offers compute resources, and which is not part of a subnetwork, but instead can be used by multiple subnetworks. The 6G core network might be involved in provisioning of the compute resources.
- **6G core network (6G CN):** The 6G core network comprises all necessary network functions to run, operate and manage the parent network. It might also include functionality to manage and operate subnetworks associated to the parent network. Subtypes: Public network and non-public network (enterprise or campus). A non-public network can provide a dedicated 6G core network to a certain scenario, such as an industrial factory.

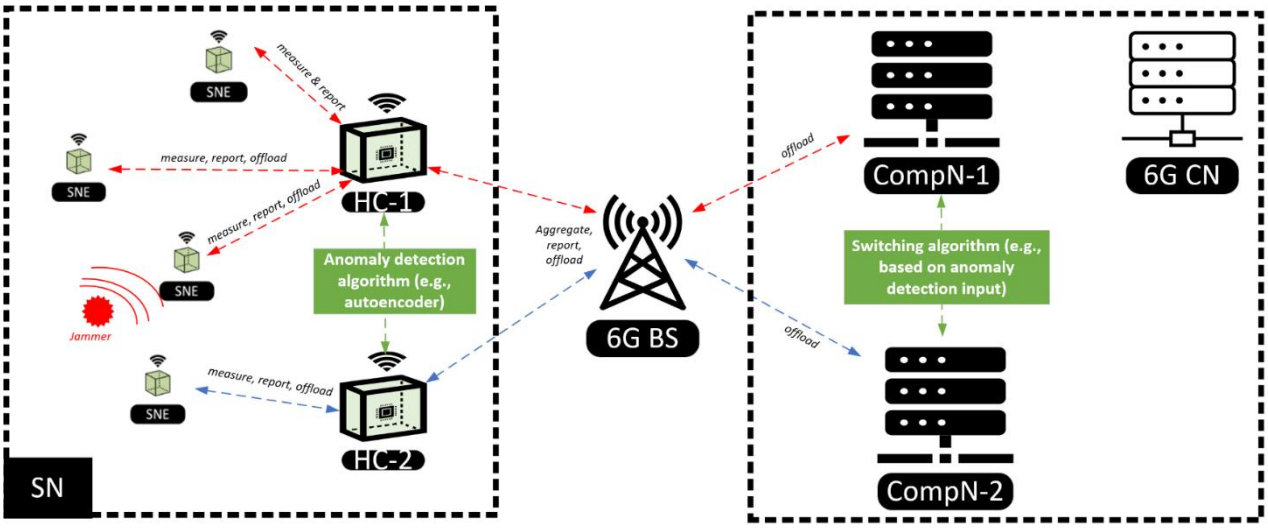

FIGURE 26. HIGH-LEVEL ARCHITECTURE DIAGRAM OF THE PROPOSED DEMONSTRATOR.

3.7.4 HW AND/OR SW REQUIREMENTS

The proposed demonstration requires the following HW and software: 1) HW requirements include NUCs, USRPS, Quectel modem; 2) SW requirements include Python environment, Keras, Linux/Windows.

3.7.5 APPLICABLE KPIS DEFINITION/PRESENTATION

In the demonstration, we aim to have a Grafana front-end to depict metrics (real-time or close to real-time). A set of potential metrics used as KPI may be captured with the PoC, as listed below:

- **Packet error rate (PER)**: we measure the packet error rate at physical layer, defined as the ratio of packet failed to be decoded against the total transmitted packet, with and without the jammer resilient feature, under the same interference scenario.
- **Throughput**: we measure the average amount of transferred information in a defined period between devices, and in the subnetwork.
- **Latency**: we measure on average the time it takes when a packet is prepared in the sender's application layer till it arrives at the receiver's application layer, with and without the jammer resilient feature, under the same interference scenario.
- **Received Signal Strength Indicator (RSSI):** a measurement of the power present in a received radio signal. Which is an indication of the power level being received by the receiving radio after the antenna and possible cable loss.
- **Link Quality Indicator (LQI):** are proprietary numbers that give an indication of how good a communication channel is for transmission and correct reception of signals, usually it is used to detect interfering signal.
- **False positive rate (FPR):** The false positive rate is calculated as the ratio between the number of negative events wrongly categorized as positive (false positives, wrong alarms of detection a jammer) and the total number of actual negative events (regardless of classification).
- **True positive rate (TPR)** also defined as sensitivity, which represents the probability of a positive test result, conditioned on the individual truly being positive.

3.7.6 BASELINE DEFINITION

Since the proposed demonstration aims to capture the benefit of detecting jammers and transmitting jamming information towards the 'umbrella' network for improved management of traffic (e.g., switching between different computational or traffic serving nodes), than our baseline is simply given by the performance obtained when this information is not being timely transmitted. Further, we will explore how parameter tuning of the anomaly detection algorithm impacts the jamming detection performance in terms of timing and accuracy, which will have an impact on the overall performance monitored in the demo.

3.7.7 DEMONSTRATION SCENARIO

The demonstration scenario will follow the steps outlined below:

1) Training of anomaly detection unit (e.g., autoencoder implementation) with diverse datasets derived either from measurements or from model distributions.
2) Testing anomaly detection unit on unseen data and parameter tuning.
3) Preliminary integration between the anomaly detection unit and the AdvenEdge as depicted in the high-level architecture.
4) Full integration by transmitting jamming information from the subnetwork to the 'umbrella' network and execution of the switching step within the 'umbrella' network.
5) Performance monitoring and adjustments.

4 CONCLUSIONS

In this deliverable, we have presented our methodology and an initial description of the PoCs to be implemented in WP5 of 6G-SHINE. Specifically, we are targeting seven PoCs: Low latency channel emulator (addressing TC2), Latency aware MAC access (addressing TC11), Jamming resilient PHY (addressing TC6), Intra-subnetwork macro-diversity (addressing TC8), Centralized RRM (addressing TC13), Centralized/distributed interference management (address both TC12 and TC13), Jamming detection using anomaly detection (addressing TC15). For each PoC, we have presented the general architecture, the hardware and software platform, targeted KPIs and intended demonstration scenarios. Identified KPIs are to large extent the same as in the simulation studies but need to be tailored to the specific evaluation setup in laboratory conditions.

This deliverable reflects the work done in Task 5.1, where the PoCs are defined. Initial implementation will continue in Task 5.2, and performance will be verified against the identified KPIs. Possibly, some of the KPIs may be refined according to the definitions given in WP2 and presented in deliverable D2.2 (submitted at the same time as this deliverable). The work in Task 5.2 will be reported in deliverable D5.2, due by December 2024, and will include a more detailed description of the developed procedures, and connection with the work carried out in the other technical WPs.

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